**Lab 4 Report**

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alu\_top– This top module contains the parametrized ALU, which has BW instances of the 1 bit ALU. There is two BW bit inputs a and b, an input cin, an input opcode, and two outputs sum & cout. The input cin is either 0 or 1. A 0 cin is used for addition, while a 1 cin is used for subtraction, since a 1 is added to the negation of b, to get the 2’s complement. The opcode is used to select the particular function using the mux. The sum output contains the final output of the ALU, and the cout, is used in the case of a cout for addition or subtraction. There is d flip flops used to store the output of the mux in a register, and produce the output from the register.

alu\_para – This is the parametrized ALU, which is made from the 1 bit alu module, for inputs which have bit sizes of BW.

alu- This module contains 1 bit inputs a and b, and the different functions are performed on these inputs. This is a submodule of the ALU top module, and hence is the building block for the n-bit ALU.

adder\_param – This module does parameterized addition of two inputs, and is a sub module of the 1 bit ALU. It is used for the addition function in the ALU.

alu\_sub – This module uses cin as 1 to subtract inputs a and b, and uses the module FA\_str, which is a full adder to subtract.

FA\_str – This module is the full adder, which produces a sum and a cout from two inputs.

dff – this is the d-flip flop module, which has an input d and an output q.

Verification\_nbit – This uses behavioral Verilog to test the outputs of our ALU.

